DETAILED ACTION

1. Claims 1-8 are pending in this office action and presented for examination. Claims 1-5 are newly amended by amendment filed 8/9/2011.

Claim Objections

2. Claims 1-8 are objected to because of the following informalities. Appropriate correction is required.

3. In claim 1, line 2, the dash should be deleted.

4. In claim 1, line 14, “the most remote cluster” should be “a most remote cluster” as it is not necessarily inherent that there exists a "most remote" cluster, as several remote clusters may be separated from the instruction unit by a same distance.

a. Claims 2-4 are objected to for failing to alleviate the objection of claim 1 above.

5. In claim 5, line 14, “the most remote cluster” should be “a most remote cluster” as it is not necessarily inherent that there exists a "most remote" cluster, as several remote clusters may be separated from the instruction unit by a same distance.

b. Claims 6-8 are objected to for failing to alleviate the objection of claim 5 above.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 1 recites the limitation "one or more additional pipeline registers" in line 9. However, the remainder of the claim does not recite any other pipeline registers. Due to the use of the limitation "additional", it is indefinite as to whether the claimed clustered instruction level parallelism processor necessitates other pipeline registers besides the "one or more additional pipeline registers". Also see col. 1, lines 11-12, which recites of "the number of additional pipeline registers".

9. Claim 1 recites the limitation "a high clock frequency" in line 13. It is indefinite as to what threshold must be passed such that a clock frequency would be considered to be a "high" clock frequency.

c. Claims 2-4 are rejected for failing to alleviate the rejection of claim 1 above.

10. Claim 5 recites the limitation "one or more additional pipeline registers" in line 9. However, the remainder of the claim does not recite any other pipeline registers. Due to the use of the limitation "additional", it is indefinite as to whether the claimed clustered instruction level parallelism processor necessitates other pipeline registers besides the "one or more additional pipeline registers". Also see col. 5, lines 11-12, which recites of "the number of additional pipeline registers".

11. Claim 5 recites the limitation "a high clock frequency" in line 13. It is indefinite as to what threshold must be passed such that a clock frequency would be considered to be a "high" clock frequency.

d. Claims 6-8 are rejected for failing to alleviate the rejection of claim 5 above.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

14. Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108) each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these

are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108).

However, Batten does not disclose of one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the respective distances between said instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster.

On the other hand, Nickolls does disclose of one or more additional pipeline registers arranged in control connections to a remote cluster of a plurality of clusters, depending on the respective distances between an instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

15. Consider claim 2, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

16. Consider claim 3, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

17. Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108) each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108).

However, Batten does not disclose of one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the respective distances between said instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster.

On the other hand, Nickolls does disclose of the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 20, lines 11-15, discloses of pipeline registers in the paths connecting different processing elements; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

18. Consider claim 6, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

19. Consider claim 7, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

20. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

21. Consider claim 4, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

22. Consider claim 8, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

Response to Arguments

23. Applicant argues on pages 7-8 that Nickolls is not analogous art because it relates to transmission of information through so-called massively-parallel Single Instruction Multiple Data (SIMD) computing machines and not a clustered Instruction Level Parallelism processor as claimed, and that it is thus not seen why one skilled in the art would look to the elements of a massively-parallel Single Instruction Multiple Data (SIMD) computing machine, although similar sounding, for use in a clustered Instruction Level Parallelism processor.

However, as conveyed in the previous office action, the examiner's combination did not entail the insertion of Nickolls' elements of a massively-parallel Single Instruction Multiple Data (SIMD) computing machine into the system of Batten. Rather, the examiner's combination only entailed the use of pipeline registers into already existing connections. The use of pipeline registers to increase the bit flow of a long path is applicable regardless of the overall environment in which that path resides, and thus its usefulness is not exclusive to Nickolls overall massively-parallel SIMD computing machine.

24. Applicant argues on page 8 that "[f]urther, Applicant respectfully submits that the Office Action has used impermissible hindsight to reject claims under 35 U.S.C. § 103(a). The Federal Circuit in In re Rouffet stated that virtually all inventions are combinations of old elements. Therefore an Examiner may often find many elements of a claimed invention in the prior art. To prevent the use of hindsight based on the

invention to defeat patentability of the invention, the Examiner is required to show a motivation to combine the references and further a motivation to modify the combination to justify a finding of obviousness. Appellants respectfully submit that the Office Action has not met this burden."

However, as conveyed in the previous office action, examiner has provided a motivation in the rejection above. Namely, the teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it is unclear as to why applicants submit that the Office Action has not met this burden.

25. Applicant argues on page 8 that "[t]he mere fact that the prior art device could be modified so as to produce the claimed device, is not a basis for an obviousness rejection unless the prior art suggested the desirability of the modification. See, In re Gordon, 733 F.2d 900, 902 (Fed, Cir. 1984); and In re Laskowski, 871 F.2d 115, 117 (Fed. Cir. 1989). The only suggestion that can be found anywhere for making the modification appears to come from the present patent application itself."

However, as previously noted, examiner has provided a motivation in the rejection above. Namely, the teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it is unclear as to why applicant states that the only suggestion that can be found anywhere for making the modification appears to come from the present patent application itself.

26. Applicant argues on pages 8-9 that "[t]he Office Action further indicates that 'Nickolls increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.' However, this is a different problem than the present invention, and it is unclear why one skilled in the art would look to the reasons there is a need to increase the bit flow rate of the path in a so-called massively-parallel Single Instruction Multiple Data (SIMD) and use them for a clustered Instruction Level Parallelism processor. One of the problems the current invention solves is that of enabling higher clock frequencies, since the clock period is not limited by the longest delay in control signals due to the longest distance between the instruction unit and the most remote cluster.

However, the problem that Nickolls addresses is not different than the present invention. In Nickolls, the insertion of pipeline registers in the message routing paths increases the bit flow path rate of the path, thereby allowing more bits per unit time to be processed. Meanwhile, the problem that the current invention is argued to solve is that of enabling higher clock frequencies, which, in a processor, typically entails processing more data per unit time. Therefore, both Nickolls and the current invention are directed toward sending more signals per unit time via the use of pipeline registers such that more signals can ultimately be processed per unit time.

27. Applicant argues on page 9 that applicant can [find] nothing in Batten or Nickolls, alone or in combination, that teaches the limitations of "one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the respective distances between said instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster."

However, Nickolls does disclose of one or more additional pipeline registers arranged in control connections to a remote cluster of a plurality of clusters, depending on the respective distances between an instruction unit and said plurality of clusters, the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires). Note that when the teaching of Nickolls is applied to the invention of Batten, the clusters which receive instructions from the instruction unit would then be able to operate at a higher clock frequency as they are receiving instructions faster. Just as the well-known concept of an instruction pipeline enables a higher clock frequency to be used in order to increase instruction throughput (as an instruction then only needs to traverse a stage of the pipeline, rather than the

entire pipeline, in any given cycle, enabling the cycles to be shorter and thus the frequency to be higher), so too would the system of Nickolls be enabled to operate at a higher clock frequency, as the instructions sent to the cluster would only have to traverse a portion of the control connection per cycle rather the entire control connection due to the pipeline registers, enabling the cycles to be shorter and thus the frequency to be higher. Examiner again notes that the use of pipeline registers to increase the bit flow of a long path is applicable regardless of the overall environment in which that path resides, and thus its usefulness is not exclusive to Nickolls overall massively-parallel SIMD computing machine, and can reasonably be applied to Batten wherein the path is the path from the instruction unit to the clusters.

28. Applicant on page 10 argues claims 2-4 and 6-8 by referencing the arguments to the independent claims discussed above.

Consequently, examiner's response to arguments with regard to the independent claims is likewise applicable to claims 2-4 and 6-8 above.

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH VICARY whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Friday, 7:00 a.m. - 3:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Keith Vicary/
Primary Examiner, Art Unit 2183